**University of Virginia**

**Charles L. Brown Department of Electrical and Computer Engineering**

**Project SRAM - Design Review 1**

Report to PICo Review Board

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**SUBJECT:** Progress on designing a 1Mb low-power SRAM

                  For the past several weeks our team has been designing and simulating the workings of SRAM.  We started by simulating a simple six transistor bit cell.  The design for the 6T cell is based on the first problem of homework three and in class knowledge of 6T bitcell.  This design was chosen for its simplicity and ease of understanding, both of which have helped the group gain a greater understanding of the operation of SRAM.  Not all of the original design could be used however, the original lacks any sizing data and has no sense amplifiers.  The lack of sense amplifiers does not affect the operation of the cell, but will need to be included later on so that the actual physical implementation of the SRAM can function properly.  Transistor sizing was based off of simulation results, specifically to meet the pull-up and cell ratio constraints for SRAM to operate correctly at Vdd=2.5V and T=27C.  Both the multiplexers and decoders are implemented using CMOS logic but transmission gates might be used later after more research is done. We plan on implementing the SRAM as a collection of 64 blocks, each composed of 256 rows and 64 columns with a word size of 32 bits, as suggested by the previous team two years ago.

We had originally planned to implement each component using SKILL, but due to unexpected circumstances (missing library & wiki being down), we were not able to do so.

For the proposal, we still need to do a lot of research on the extra features. We have borrowed two textbooks from the library among many that we found. We have also found some good papers on ieeexplore. Some proposed modifications are: current sense amps, changing Vsb to alter Vthreshold, keeping the number of rows per block low, changing the size of the transistors, finding an optimal Vdd, and reducing leakage current wherever possible. We also intend to look into the previous team’s implementations of sleep mode and error correcting code. All modifications will be done with the goal of minimizing energy consumption so as to achieve a high score metric for the project.  The use of current sense amps would allow for smaller changes in the bitlines to be detected.  Keeping the number of rows per block low means that the number of cells per bitline is kept low.  Both modifications prevent the bitlines from having to charge and discharge as much, reducing energy wasted per cycle.  Decreasing the source-bulk voltage has the effect of decreasing the threshold voltage of the transistor.  Having a smaller threshold voltage reduces the supply voltage required, and may save a lot of energy.  Sizing the transistors optimally should reduce the amount of current used by the transistor.  Dealing with leakage currents will consist of finding leakage in our design and researching ways to minimize it.

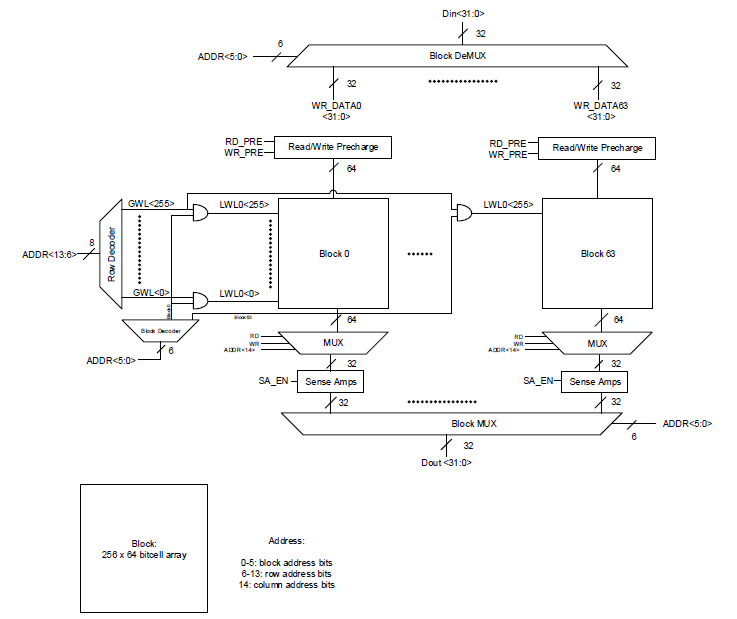
Following the proposal, we will work on the implementation & testing specified in the proposal as well as optimization e.g. process corner check & timing. This will be done over the course of several weeks with each of us taking a specific design to implement in Cadence&Ocean and extend using Skill.  To do this, each group member will be expected to complete the tutorials on using Skill and Ocean.  The rough working design with all additions implemented will then need to be tested and modified to operate over the operating conditions specified in the project assessment (T=0, 27, 100C) (Vdd=1.0,1.1,1.2V). We will keep in mind of the goal to minimize power (and reasonable values for size and speed). As a result of dividing the work, each member will also have to continue doing research.

**Specific tasks completed (some copied from previous design review). The documentation for each one is attached.**

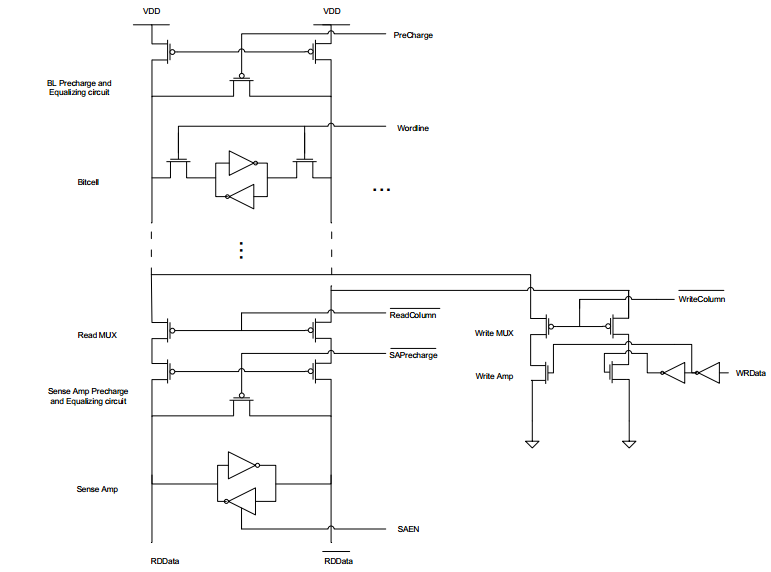
1. Block Diagram showing arrangement of major SRAM components
2. Gate level netlist of one block of the array
3. Timing diagram for the memory specifically showing the read and write operations
4. A functional bit-cell layout
5. Simulation results
   1. Process Corner: 1.2 V 50 C
6. Schematics & Testing of individual components

**Acknowledgements:**

Without the guidance and support of Professor Benton Calhoun, Professor Aatmesh Shrivastava, and Divya Akella, this 1st design review would not have been possible. We are very grateful for their help and communication with us throughout the process.

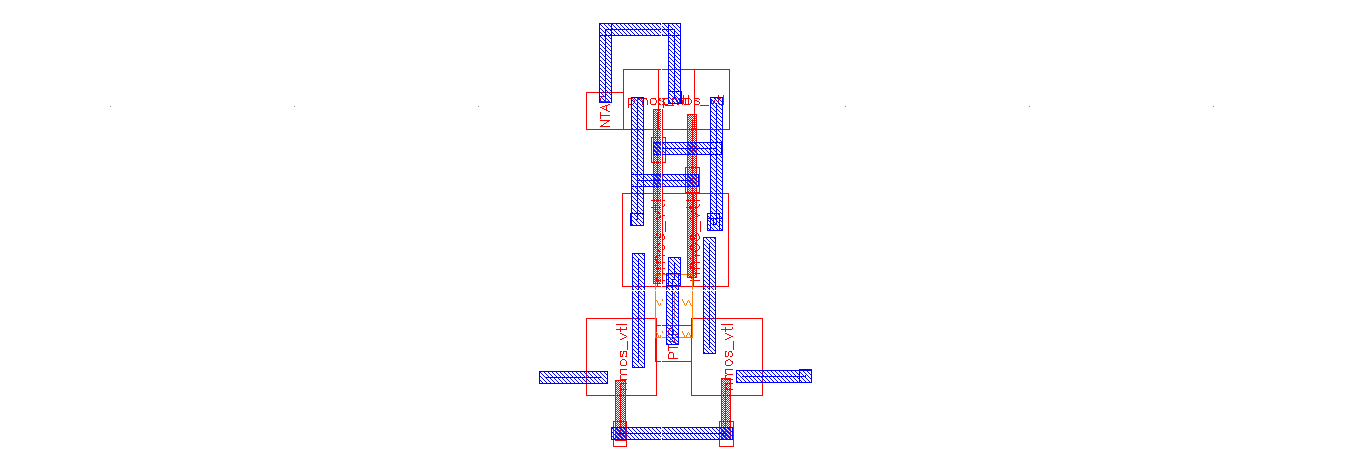
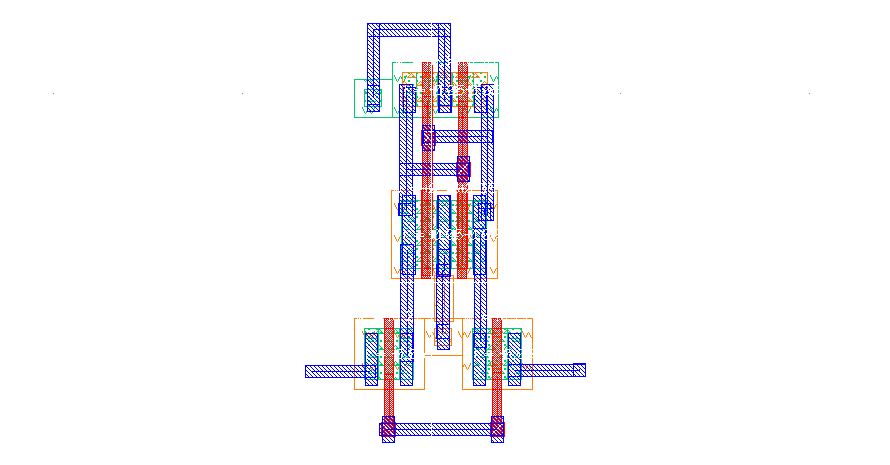
1)

2) Similar to the one from two years ago?

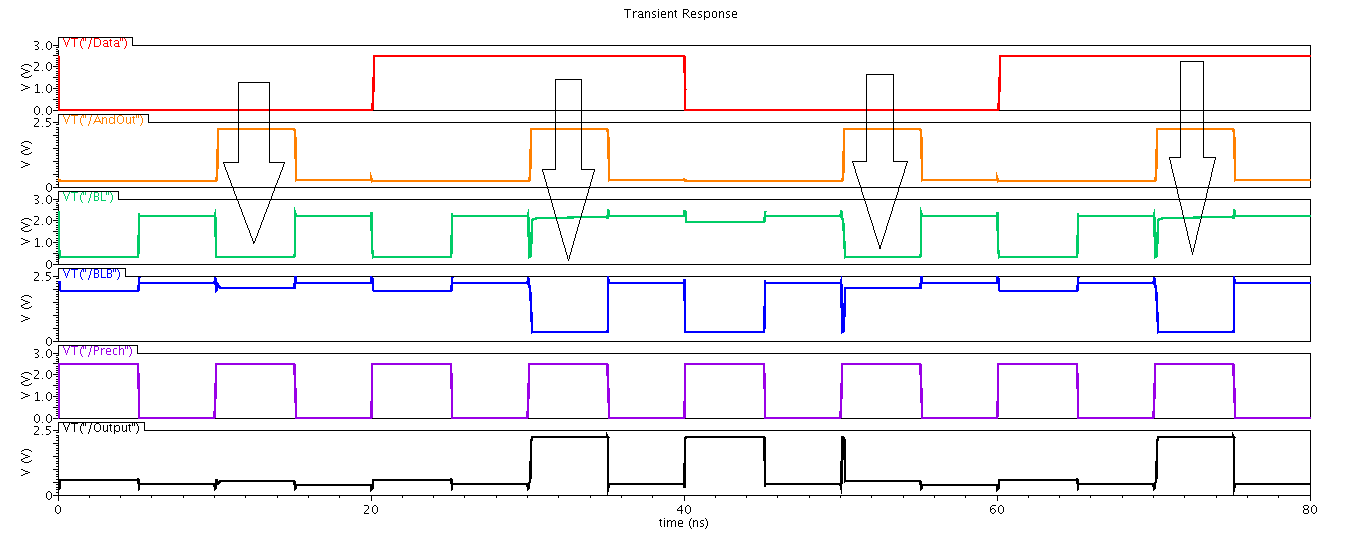


3) Attached separately (pdf file is too large).

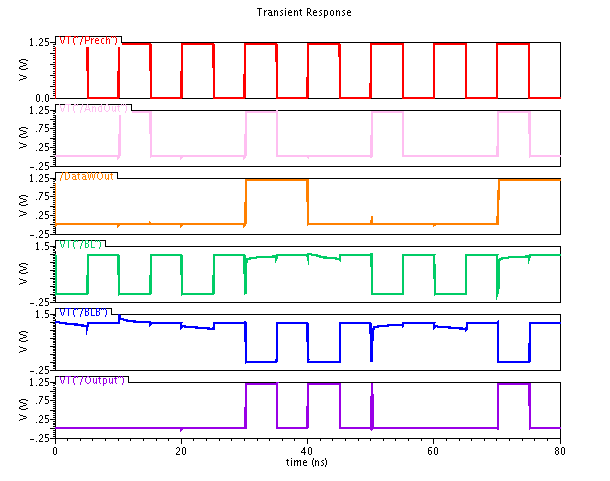
4)



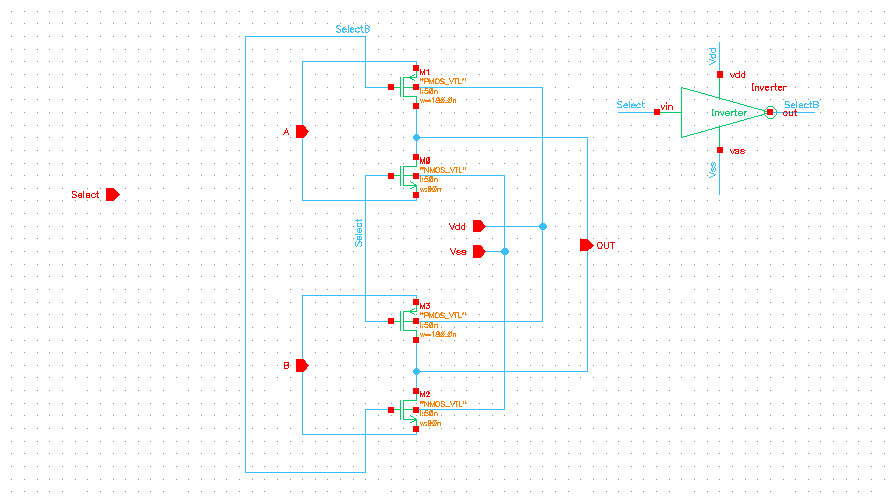
5) Essentially SRAM is reading when precharge is on (since there is just a single bit—no address line). SRAM writes the data into BL when AND gate of precharge & write is 1 (labeled with arrows).

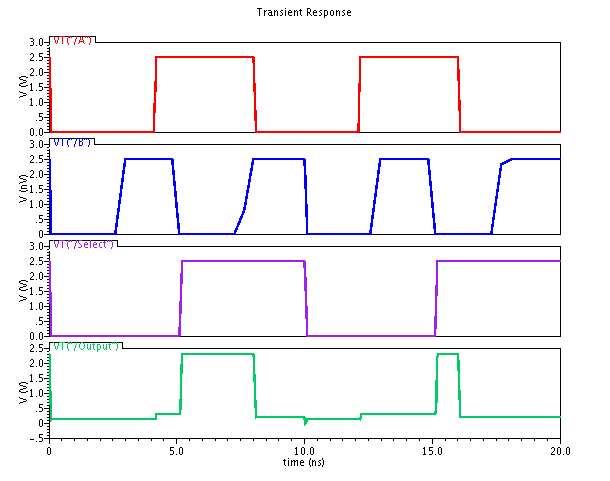


6) Process Corner Test @ 50 C, 1.2 V

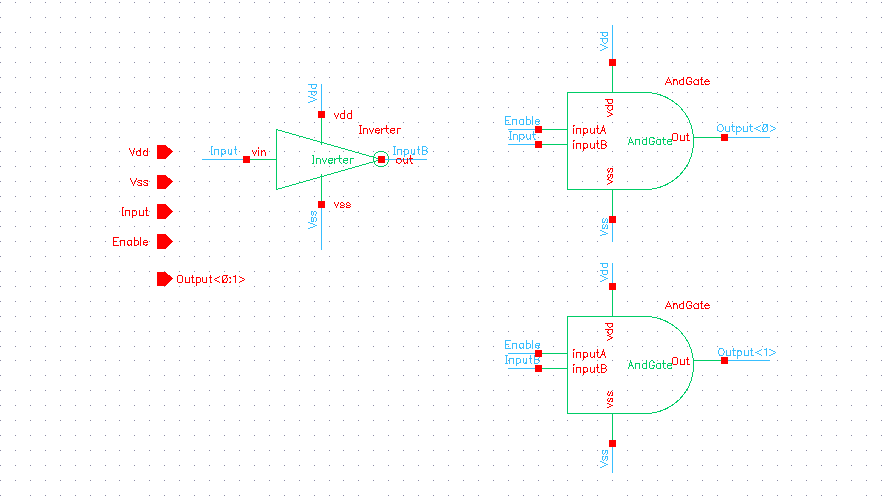


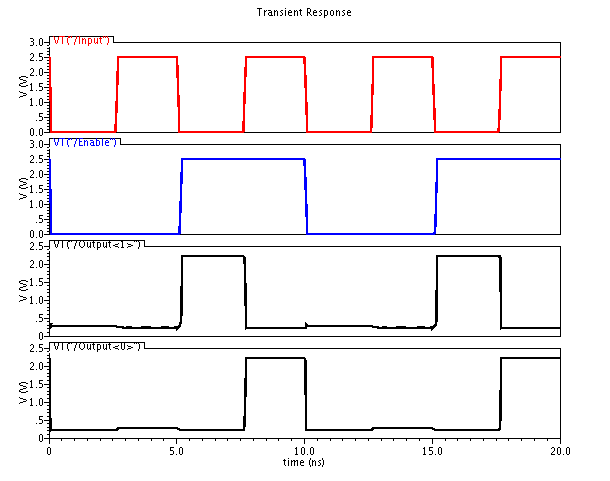
MUX



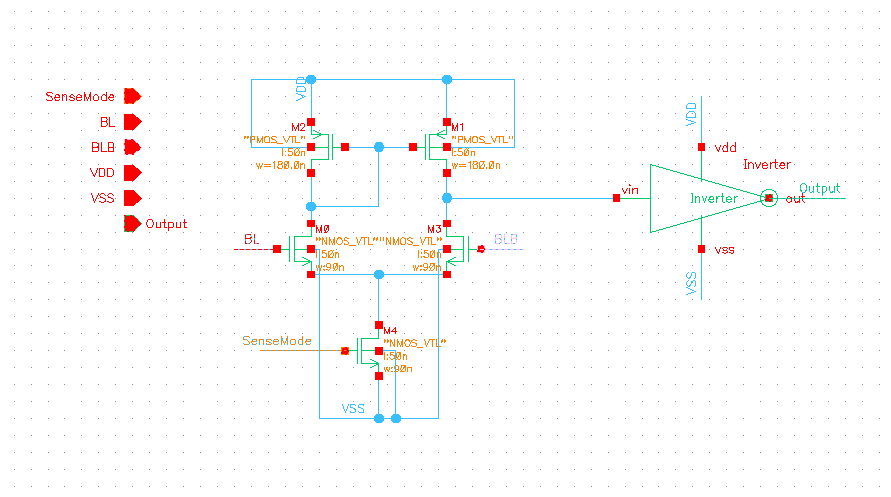


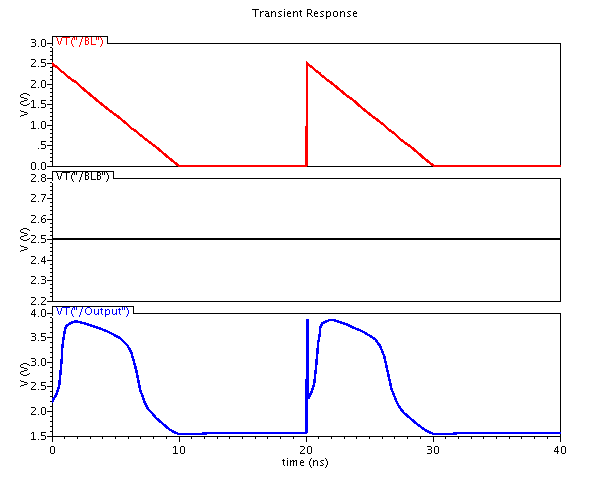
Decoder



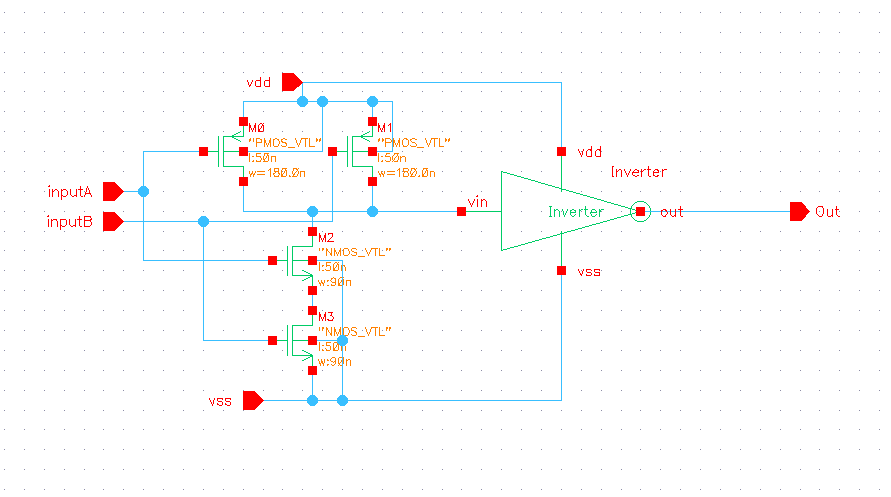


Sense Amplifier

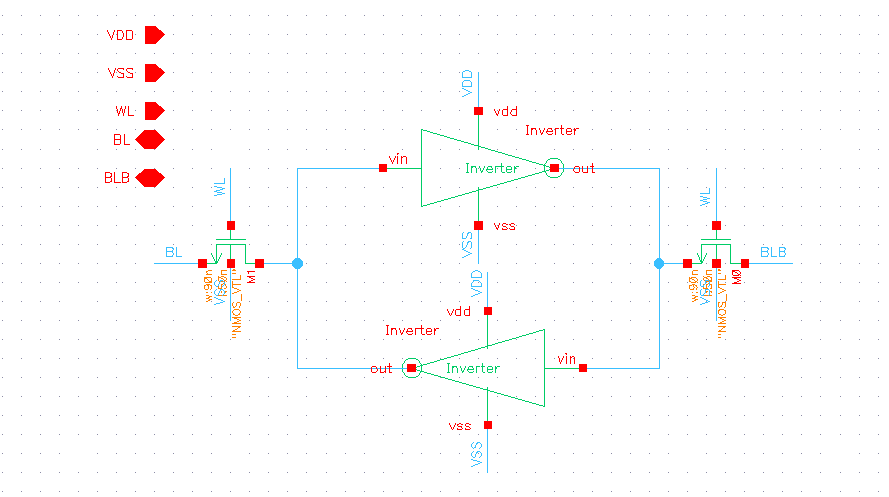




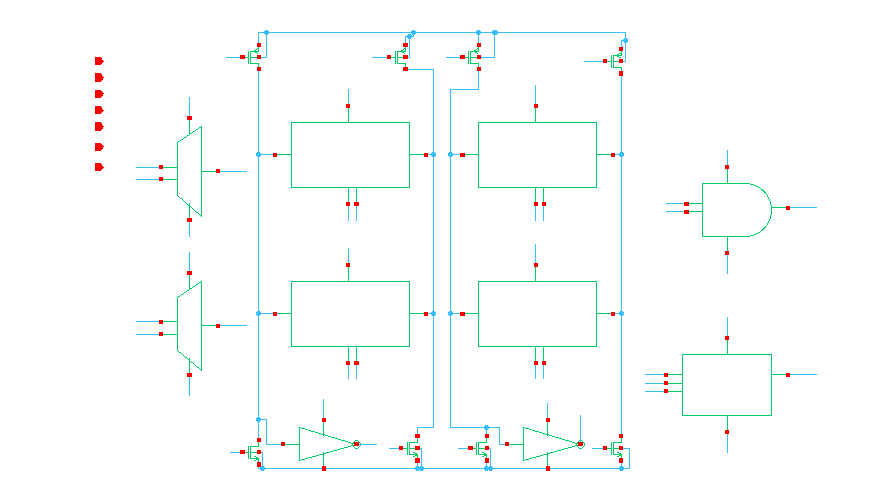
And Gate



Bit Cell



2x2 SRAM



1 Bit SRAM TEST Bench:

